VERIFICATION OF TRANSLATION

I, Jin-Seok Kim of 1-170, Soonhwa-Dong, Jung-Gu, Seoul, Republic of Korea, hereby declare that, to the best of my knowledge and belief, the attached is a true English translation of the certified copy of the Korean Patent Application No. 10-2002-0040702.

Signature of translator

Jin Seok Kim

Dated this 11th day of August, 2004

(Translation)

KOREAN INTELLECTUAL PROPERTY OFFICE

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Applicant(s): HYNIX SEMICONDUCTOR INC.

COMMISSIONER

[ABSTRACT]

[Summary]

Disclosed is a method of manufacturing semiconductor devices. In the process of simultaneously forming a high voltage device and a low voltage device, a photoresist film for patterning a gate oxide film in a high voltage device is removed in a wet mode using a solvent. The polysilicon film used as the gate electrode is then formed without applying vacuum. It is thus possible to increase reliability of the gate oxide film, and prevent damage of the gate oxide film due to ozone plasma and penetration of a grain protrusion of the polysilicon film into the gate oxide film. Accordingly, a breakdown voltage characteristic of the gate oxide film could be improved.

[Representative Drawing]

Fig. 3

[Index Word]

High Voltage Device, Low Voltage Device, Photoresist Film, Solvent, Polysilicon, Breakdown Voltage Characteristics

[SPECIFICATION]

[Title of the Invention]

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

[Brief Description of the Drawings]

FIG. 1 is a SEM photo showing that a photorest remnant remains in the process of removing the photoresist film using ozone plasma,

FIG. 2 is a graph illustrating current distribution depending on the gate voltage in case that a polysilicon film formed by applying vacuum of four times is used as a gate electrode,

FIG. 3A ~ FIG. 3D are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device according to a preferred embodiment of the present invention,

FIG. 4 is a SEM photo showing that the photoresist film is removed using a wet solvent, and

FIG. 5 is a graph illustrating breakdown voltage characteristics of a high voltage device in which the gate electrode is formed using the polysilicon film formed while applying vacuum, and a high voltage device in which a gate electrode is formed using a polysilicon film that is formed without applying vacuum.

<The Reference Numerals in The Drawings>

A: high voltage device region B: low voltage device region

11: semiconductor substrate
12: isolation film
13: first oxide film
14: photoresist film
15: second oxide film
16: polysilicon film
17: spacer
18: junction region

[Detailed Description of the Invention]

[Object of the Invention]

[Technological Background of the Invention and Description of the Prior Art]

The present invention relates to a method of manufacturing semiconductor devices, and more particularly, to a method of manufacturing semiconductor devices by which in the process of simultaneously forming a high voltage device and a low voltage device, a photoresist film for patterning a gate oxide film in a high voltage device is removed in a wet mode using a solvent, and the polysilicon film used as the gate electrode is formed without applying vacuum, whereby reliability of the gate oxide film is increased, damage of the gate oxide film due to ozone plasma is prevented and penetration of a grain protrusion of the polysilicon film into the gate oxide film is prevented, thus improving a breakdown voltage characteristic of the gate oxide film.

In semiconductor devices in which a high voltage device operating at a high voltage and a low voltage device operating at a low voltage are simultaneously fabricated, the gate oxide film in the high voltage device is formed thicker than the gate oxide film in the low voltage device. This is for improving a breakdown voltage characteristic against the high voltage.

This method of manufacturing the semiconductor devices includes the steps of thickly forming a first gate oxide film on a semiconductor substrate, removing the first gate oxide film in a low voltage device region using a photoresist film pattern, removing the photoresist film pattern using ozone plasma, and then thinly forming a second gate oxide film in the low voltage region. Next, a polysilicon film for forming the gate electrode is formed. At this time, the polysilicon film is formed by applying vacuum of several times while the polysilicon film is formed to have a given thickness. For example, in the process of forming the polysilicon film of 2000 Å in thickness, vacuum of four times is applied. At this time, vacuum is applied once every time when the polysilicon film is formed in thickness of 500 Å.

However, in the process of removing the photoresist film using ozone plasma, the photoresist film is not completely removed but the remnant remains, as shown in FIG. 1. This degrades reliability of the gate oxide film and damages the gate oxide film due to plasma.

Further, the method of forming the polysilicon film by applying vacuum of four times is good in a dopant channeling prevention characteristic. As a grain protrusion of the polysilicon film penetrates into the gate oxide film, however, an interfacial roughness between the gate oxide film and polysilicon is increased, thereby increasing the leakage current at a pre-tunneling region. This phenomenon could be known from distribution of FIG. 2. FIG. 2 is a graph illustrating current distribution depending on the gate voltage in case that the polysilicon film formed by applying vacuum of four times is used as the gate electrode. FIG. 2 illustrates the results of measuring about 25 dies.

It could be said that current is increased at the pre-tunneling region where the grain protrusion of polysilicon penetrates into the gate oxide film. Further, if the polysilicon film is formed by the above method, the process time is increased to that extent.

[Technical Means for Achieving the Object of the Invention]

An object of the present invention is to provide a method of manufacturing semiconductor devices by which a photoresist film remnant does not remain in the removal process of the photoresist film, thereby improving reliability of a gate oxide film.

Another object of the present invention is to provide a method of manufacturing semiconductor devices capable of preventing reduction in a breakdown voltage characteristic due to a grain protrusion of polysilicon.

[Structure and Operation of the Invention]

A method of manufacturing semiconductor devices according to a preferred embodiment of the present invention is characterized in that it comprises the steps of forming an isolating film at a given region of a semiconductor substrate to define a first region and a second region, forming a first oxide film on the entire structure and then removing the first oxide film in the second region using a photoresist film pattern, removing the photoresist film pattern using a solvent, implementing an oxidization process to form a second oxide film on the semiconductor substrate in the second region,

forming a polysilicon film on the entire structure and then patterning the polysilicon film to form gate electrodes in the first and second regions, respectively, and implementing an impurity ion implantation process to form junction regions at given regions on the semiconductor substrate.

In an aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed. Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

FIG. 3A ~ FIG. 3D are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device according to a preferred embodiment of the present invention,

Referring to FIG. 3A, an isolation film **12** is formed at a given region of a semiconductor substrate **11** to define a high voltage device region and a low voltage device region. An ion implantation process is then performed to form a well region. Next, the semiconductor substrate **11** is precleaned using a HF solution diluted with a mixture solution of $NH_4OH/H_2O_2/H_2O$. Thereafter, a first oxide film **13** is thickly formed on the entire structure. At this time, the first oxide film **13** is formed by oxidizing the semiconductor substrate **11** using vaporized H_2O generated by pyrolysis of oxygen and hydrogen in the furnace. Then, a photoresist film **14** of i-line series, having a thickness of about 1 μm, is formed on the first oxide film **13**. The photoresist film **14** is then patterned to

expose the low voltage device region. Thereafter, the first oxide film **13** formed on the semiconductor substrate **11** in the low voltage device region is removed by wet etch using the patterned photoresist film **14** as a mask.

By reference to FIG. 3B, the photoresist film **14** formed in the high voltage device region is removed using a solvent. The solvent may include ethylcellsoluve acetate (ECA), methylamyl ketone (MAK), ethyl pyruvate (EP), ethyl lactate (EL), 3-methylmethoxy propionate (MMP), propyleneglycomonomethyl ether (PGME), propyleneglycol-monomethylether acetate (PGMEA), ethoxyethyl propionate (EEP), and the like.

Referring to FIG. 3C, an oxidization process is implemented to form a second oxide film **15** having a thin thickness on the semiconductor substrate **11** in the low voltage device region. At this time, the first oxide film **13** is also grown by a given thickness. A polysilicon film **16** is then formed on the entire structure, wherein the polysilicon film **16** is formed by not applying vacuum and is formed at a temperature of 580～630℃ using SiH_4 gas or Si_2H_6 gas. After the polysilicon film **16** is formed, an annealing process is implemented at a temperature of 800～1000℃ in the furnace or a rapid thermal annealing equipment.

By reference to FIG. 3D, given regions of the polysilicon film **16** and the first oxide film **13** in the high voltage device region, and given regions of the polysilicon film **16** and the second oxide film **15** in the low voltage device region are etched to form first and second gate electrodes. A low concentration impurity ion implantation process is then implemented. Next, spacers **17** are formed at the sidewalls of the gate electrodes. Thereafter, a

high concentration impurity ion implantation process is implemented to form junction regions **18** on the semiconductor substrate **11**.

If the semiconductor devices are fabricated by the above process, the photoresist film is removed using a wet solvent. Therefore, particles generated during the process remain but the photoresist film remnant does not remain, as shown in FIG. 4.

Further, FIG. 5 is a graph illustrating breakdown voltage characteristics of a high voltage device **C** in which the gate electrode is formed using the polysilicon film formed while applying evaporation, and a high voltage device **D** in which a gate electrode is formed using a polysilicon film that is formed without applying vacuum.

As shown in FIG. 5, it could be seen that the high voltage device **C** has a high voltage breakdown voltage characteristic of 8V or -8V but the high voltage device **D** has a breakdown voltage of around 0V. It can be thus understood that the high voltage device **C** has a better breakdown voltage characteristic than the high voltage device **D**.

[Effect of the Invention]

As described above, as the photoresist film is removed in a wet mode using a solvent, a photoresist film remnant does not remain. Therefore, the present invention has advantageous effects that it can increase reliability of the gate oxide film and prevent damage of the gate oxide film due to ozone plasma.

Further, as the polysilicon film is formed by not applying vacuum, penetration of a grain protrusion of the polysilicon film into the gate oxide film

could be prevented. Therefore, the present invention has new effects that it can improve a breakdown voltage characteristic of the gate oxide film and shorten the process time.

What is claimed is:

1. A method of manufacturing semiconductor devices, comprising the steps of:

forming an isolating film at a given region of a semiconductor substrate to define a first region and a second region;

forming a first oxide film on the entire structure and then removing the first oxide film in the second region using a photoresist film pattern;

removing the photoresist film pattern using a solvent;

implementing an oxidization process to form a second oxide film on the semiconductor substrate in the second region;

forming a polysilicon film on the entire structure and then patterning the polysilicon film to form gate electrodes in the first and second regions, respectively, and

implementing an impurity ion implantation process to form junction regions at given regions on the semiconductor substrate.

2. The method as claimed in claim 1, wherein the first oxide film is formed thicker than the second oxide film.

3 The method as claimed in claim 1, wherein the photoresist film is formed using an i-line series photoresist material.

4 The method as claimed in claim 1, wherein the solvent includes

any one of ethylcellsoluve acetate (ECA), methylamyl ketone (MAK), ethyl pyruvate (EP), ethyl lactate (EL), 3-methylmethoxy propionate (MMP), propyleneglycomonomethyl ether (PGME), propyleneglycol-monomethylether acetate (PGMEA) and ethoxyethyl propionate (EEP).

5 The method as claimed in claim 1, wherein the polysilicon film is formed without applying vacuum and is formed using SiH_4 gas or Si_2H_6 gas at a temperature of 580 ~ 630 ℃.